IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 13 with the following amended paragraph:

The present patent application is related to co-pending and commonly owned U.S. Patent Application No. 10/038,209 ~~XX/XXX,XXX~~, Attorney Docket No. POU920010165US1, now U.S. Patent No. 6,817,000, entitled "Delay Correlation Analysis and Representation for VITAL Compliant VHDL Models", and U.S. Patent Application No. 10/038,689 ~~XX/XXX,XXX~~, Attorney Docket No. POU920010166US1, entitled "VHDL Technology Library Method for Efficient Customization of Chip Gate Delays", filed on even date with the present patent application, the entire teachings of which being hereby incorporated by reference.

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